What is claimed is:

1. A strained silicon fin structure comprising

   - an insulator substrate;

   - a silicon seed fin structure disposed on the substrate; and

   - a strained channel layer fabricated on the seed fin structure, the channel layer material having a lattice constant different than that of the seed fin material,

   whereby the channel layer strain is the result of the lattice mismatch between the channel layer material and the seed fin material.

2. A strained silicon fin structure as in claim 1 further comprising an underseed layer disposed between the seed fin structure and the substrate, the underseed layer material having a lattice constant different than that of the seed fin material, whereby the seed fin structure is under strain due to the lattice mismatch between the underseed layer material and the seed fin material.

3. A strained silicon fin structure as in claim 1 further comprising a hard mask layer on the seed fin structure.

4. A strained silicon finFET device comprising

   - an insulator substrate;

- a source and a drain sandwiching a strained channel region disposing on the substrate, the strained channel comprising
  - a seed fin structure; and
  - a strained channel layer fabricated on the seed fin structure, the channel layer material having a lattice constant different than that of the seed fin material;
- a gate dielectric layer disposed on the strained channel; and
- a gate over the strained channel and electrically isolated therefrom by the gate dielectric.

5. A strained silicon finFET device as in claim 4 wherein the seed fin structure material is silicon germanium or silicon.

6. A strained silicon finFET device as in claim 4 wherein the channel layer material is epitaxial silicon, epitaxial silicon germanium, epitaxial carbon doped silicon, or epitaxial carbon doped silicon germanium.

7. A strained silicon finFET device as in claim 4 further comprising a hard mask layer on the seed fin structure.

8. A strained silicon finFET device as in claim 4 further comprising an underseed layer disposed between the seed fin structure and the

substrate, the underseed layer material having a lattice constant different than that of the seed fin material, whereby the seed fin structure is under strain due to the lattice mismatch between the underseed layer material and the seed fin material

9. A strained silicon finFET device as in claim 4 further comprising doping implantation for the strained channel and the source and drain.

10. A strained silicon finFET device as in claim 4 wherein the source region and the drain region include a lightly doped region extending to the channel region.

11. A strained silicon finFET device as in claim 4 further comprising silicidation of the gate, source and drain.

12. A method of fabricating a strained silicon finFET device, comprising the steps of:

a) providing a silicon on insulator substrate having a silicon-containing multilayer on an insulator layer;

b) patterning the multilayer into a source region and a drain region sandwiching a seed channel region, the seed channel being a seed fin structure;

c) depositing an epitaxial channel layer onto the seed fin structure, the channel layer material having a lattice constant different than that of the seed fin material, wherein the epitaxial channel layer becomes a strained channel layer due to the lattice mismatch between the channel layer and the seed fin structure;

d) forming a gate dielectric layer on the epitaxial strained channel; and

e) forming a gate over the epitaxial strained channel.

13. A method as in claim 12 wherein the silicon on insulator substrate is an SOI substrate wherein the silicon-containing multilayer comprises a silicon layer.

14. A method as in claim 12 wherein the silicon on insulator substrate is an SGOI substrate wherein the silicon-containing multilayer comprises a silicon germanium layer.

15. A method as in claim 14 wherein the germanium content of the silicon germanium seed fin is between 10% to 100%.

16. A method as in claim 12 wherein the epitaxial channel layer is a silicon layer, a silicon germanium layer, a carbon doped silicon layer, or a carbon doped silicon germanium layer.

17. A method as in claim 12 wherein the patterning of the source, drain and channel regions from the multilayer comprises the steps of:

b1) providing a patterned mask on the multilayer;

b2) patterning the multilayer according to the patterned mask to define source, drain and channel regions; and

b3) removing the patterned mask.

18. A method as in claim 12 further comprising a step c1 after step c:

c1) doping the channel region.

19. A method as in claim 12 wherein the formation of the gate comprises the steps of:

e1) depositing a gate material layer;

e2) doping the gate material layer;

e3) providing a patterned mask on the gate material layer;

e4) patterning the gate material layer according to the patterned mask to define the gate; and

e5) removing the patterned mask.

20. A method as in claim 12 further comprising a step f after step e:

f) forming lightly doped region (LDD) and halo regions between the channel region and the source and drain regions.

21. A method as in claim 12 further comprising the following steps after step e:

g) forming dielectric spacers between the gate and the source and drain regions.

h) doping the source and drain regions.

i) forming salicide of the gate, source and drain regions.

22. A method as in claim 12 wherein the multilayer comprises

a first silicon-containing layer; and

a second silicon-containing layer, the second silicon-containing layer material having a lattice constant different than that of the first silicon-containing layer, wherein the second silicon-containing layer becomes a strained layer due to the lattice mismatch between the second silicon-containing layer and the first silicon-containing layer.

23. A method as in claim 22 wherein the multilayer is formed by

providing a silicon on insulator substrate having a first silicon-containing layer on an insulator; and

depositing a second silicon-containing layer on the silicon on insulator substrate, the second silicon-containing layer material

having a lattice constant different than that of the first silicon-containing layer.

24. A method as in claim 22 wherein the thickness of the first silicon-containing layer is between 5 nm to 20 nm.

25. A method as in claim 22 wherein the first silicon-containing layer is a silicon layer and the second silicon-containing layer is a silicon germanium layer

26. A method as in claim 25 wherein the germanium content of the silicon germanium layer is between 10% to 50%.

27. A method as in claim 12 wherein the top most layer of the multilayer comprises a hard mask layer.

28. A method as in claim 12 wherein the height of the seed fin structure is between 10 nm to 200 nm.

29. A method as in claim 12 wherein the width of the seed fin structure is between 5 nm to 100 nm.

30. A method as in claim 12 wherein the thickness of the strained channel layer is between 5 nm to 15 nm.